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| APPLICATION NO.          | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--------------------------|-------------|----------------------|---------------------|------------------|
| 10/849,864               | 05/21/2004  | Jae Shin Yu          | HI-0202             | 8704             |
| 34610                    | 7590        | 02/13/2008           | EXAMINER            |                  |
| KED & ASSOCIATES, LLP    |             |                      | FUJITA, KATRINA R   |                  |
| P.O. Box 221200          |             |                      | ART UNIT            |                  |
| Chantilly, VA 20153-1200 |             |                      | PAPER NUMBER        |                  |
|                          |             |                      | 2624                |                  |
|                          |             |                      | MAIL DATE           |                  |
|                          |             |                      | DELIVERY MODE       |                  |
|                          |             |                      | 02/13/2008          |                  |
|                          |             |                      | PAPER               |                  |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

**Application No.**

10/849,864

**Applicant(s)**

YU ET AL.

**Examiner**

Katrina Fujita

**Art Unit**

2624

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 26 November 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1,3-11 and 13-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3-11 and 13-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Amendment***

1. This Office Action is responsive to Applicant's remarks received on November 26, 2007. Claims 1, 3-11, 13-18 and newly added 19 and 20 remain pending.

### ***Specification***

2. The previous specification objection has been withdrawn in light of Applicant's remarks.

### ***Claim Suggestions***

3. The previous claim suggestions have been withdrawn in light of Applicant's amendment.

### ***Claim Objections***

4. The previous claim objections have been withdrawn in light of Applicant's amendment.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1, 3-5 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fukunaga et al. (US 6,683,988), Hayashi et al. (US 6,694,040) and common knowledge in the art.

Regarding **claim 1**, Fukunaga et al. discloses a video communication system ("picture transmission system" at col. 2, line 40) comprising a video encoder ("coding apparatus" at col. 4, line 12) and a video decoder ("decoding apparatus" at col. 5, line 42), wherein the video encoder includes:

a data hiding processing unit (figure 4, numeral 109) for performing a data hiding operation ("frame number is included in the end-of-modification information" at col. 5, line 40) on an error information ("decoding error signal specifies a frame number" at col. 4, line 62) received from the video decoder ("receives decoding error signals from the

decoding apparatus" at col. 4, line 61), and transmitting a processed error information ("end-of-modification information" at col. 5, line 39) to the video decoder, the processed error information having a hidden data ("frame number" at col. 5, line 40); and

a first error concealment processing unit (figure 4, numeral 107) for performing an error concealment ("replaces each designated block in frame N with the corresponding block from the preceding frame" at col. 5, line 6) with reference to the error information, wherein the first error concealment processing unit performs the error concealment for a frame that corresponds to the error information received from the video decoder ("receives a frame number (denoted by N below) and one or more block numbers" at col. 5, line 2), the error concealment generating a reference frame ("modifies the picture data stored in the reference-picture memory" at col. 6, line 29; "reference frame" at col. 6, line 13) on which the data hiding operation is performed ("replacing the block in which the error occurred with the corresponding block in the preceding frame" at col. 6, line 30),

wherein the video decoder includes:

a data extraction unit (figure 5, numeral 202) for extracting an information ("frame and block number" at col. 6, line 6) on an error frame ("frame and block number of the block in which the error occurred" at col. 6, line 6), providing the extracted frame information to the video encoder ("sends a decoding error signal to the coding apparatus" at col. 6, line 17), and a second data extraction unit (figure 5, numeral 208) extracting the hidden data ("decides which frame contained the error for which the modification was made" at col. 6, line 50) provided from the video encoder; and

a second error concealment processing unit (figure 5, numeral 206) for performing an error concealment ("replacing the block in which the error occurred" at col. 6, line 30) with reference to the extracted hidden data ("receives end-of-modification information from the end-information receiver" at col. 6, line 39).

Fukunaga et al. does not disclose embedding a number of bits of the error information into a frame currently being encoded, said embedding performed by modifying at least one parameter of the frame currently being encoded and extracting the hidden data including the embedded number of bits provided from the video encoder.

Hayashi et al. teaches a method in the same field of endeavor of encoding image data ("encoding digital-watermark information in image data" at col. 15, line 18) including a data hiding operation including embedding a number of bits of the error information into a frame currently being encoded ("an error correction encoding circuit 1904 error correction encodes the digital-watermark information 1507 to generate error correction encoding digital-watermark information" at col. 15, line 21), said embedding performed by modifying at least one parameter of the frame currently being encoded ("control unit 1511 can freely set the value of the quantizing step used in the quantizing circuit 1902 in correspondence with the feature of image data for one block. The value of the quantizing step used in the quantizing circuit 1902 is externally supplied as one of the extracting parameter information required" at col. 16, line 2) and extracting the hidden data including the embedded number of bits provided from the video encoder (figure 22, numeral 2203; "extracting 1-bit embedded information" at col. 17, line 30).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to utilize the error information embedding and extraction of Hayashi et al. to hide the error frame number in the coded frame of Fukunaga et al. such that the information "can be embedded without deteriorating the original image" (Hayashi et al. at col. 16, line 34).

The Fukunaga et al. and Hayashi et al. combination does not disclose that the data extraction unit and the second data extraction unit form a single unit.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to combine together the decoding unit and the end-information receiving unit of the Fukunaga et al. and Hayashi et al. combination to enable a more efficient utilization of the decoder space.

Regarding **claim 3**, the Fukunaga et al., Hayashi et al. and common knowledge in the art combination discloses a video communication system wherein the processed error information is a frame number that corresponds to the reference frame ("frame number" Fukunaga et al. at col. 5, line 29), and wherein the number of bits embedded by modifying said at least one parameter of the frame currently being encoded is indicative of the frame number (as the data embedding is employed to hide the error frame number, the embedded data is indicative of this information).

Regarding **claim 4**, Fukunaga et al. discloses a video communication system wherein the extracted frame information is an information ("error signal to report all of

the erroneous blocks” at col. 6, line 24) that represents whether or not the error occurs in each group of blocks (“multiple blocks in the same frame” at col. 6, line 22).

Regarding **claim 5**, Hayashi et al. discloses that said at least one parameter is at least one of a quantization parameter corresponding to the frame currently being encoded (“control unit 1511 can freely set the value of the quantizing step used in the quantizing circuit 1902 in correspondence with the feature of image data for one block. The value of the quantizing step used in the quantizing circuit 1902 is externally supplied as one of the extracting parameter information required” at col. 16, line 2) or a level value of a block to which a discrete cosine transform is performed.

Regarding **claim 19**, Hayashi et al. discloses that the data hiding operation is performed before quantization of the frame currently being encoded (as seen in figure 19, the data hiding is performed in 1904 and then proceeds to the quantizer 1902).

7. Claims 15-17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fukunaga et al. and Hayashi et al.

Regarding **claim 15**, Fukunaga et al. discloses a video coding method (“each picture in the series being coded and decoded” at col. 2, line 42) comprising the steps of:

extracting an error frame information (“frame and block number” at col. 6, line 6) at a video decoder (“decoding apparatus” at col. 5, line 42) during a decoding and providing the extracted error frame information from the video decoder (“receives



decoding error signals from the decoding apparatus" at col. 4, line 61) to a video encoder ("coding apparatus" at col. 4, line 12);

performing an error concealment ("replaces each designated block in frame N with the corresponding block from the preceding frame" at col. 5, line 6) at the video encoder based on the extracted error frame information provided from the video decoder ("receives a frame number (denoted by N below) and one or more block numbers" at col. 5, line 2), the error concealment generating a reference frame ("modifies the picture data stored in the reference-picture memory" at col. 6, line 29; "reference frame" at col. 6, line 13),

performing a data hiding operation ("frame number is included in the end-of-modification information" at col. 5, line 40), based on the reference frame ("reference-relationship memory 108 stores the information received from the coding unit 102, indicating which blocks in the preceding frame were used as reference blocks" at col. 5, line 22), and

transmitting ("passes this frame number to the coded-data transmission unit" at col. 5, line 37) the currently encoded frame ("coded moving-picture data from the coding apparatus" at col. 5, line 49) to the video decoder; and

extracting the hidden data ("end-of-modification information is included with the received data, the coded-data receiving unit 201 supplies this information to the end-information receiving unit" at col. 5, line 53) transmitted from the video encoder at the video decoder, modifying ("modifies the picture data stored in the reference-picture memory" at col. 6, line 29) a reference frame ("reference frame" at col. 6, line 13) of a

frame ("current frame" at col. 4, line 32) that is encoded ("coded moving-picture data" at col. 5, line 49) using the extracted hidden data ("replacing the block in which the error occurred with the corresponding block in the preceding frame" at col. 6, line 30), and performing an error concealment ("replacing the block in which the error occurred" at col. 6, line 30) at the decoder.

Fukunaga et al. does not disclose embedding a number of bits of the error information into a frame currently being encoded, said embedding performed by modifying at least one parameter of the frame currently being encoded and extracting the hidden data including the embedded number of bits provided from the video encoder, transmitting the currently encoded frame containing the embedded number of bits and extracting the embedded number of bits.

Hayashi et al. teaches a method in the same field of endeavor of encoding image data ("encoding digital-watermark information in image data" at col. 15, line 18) including a data hiding operation including embedding a number of bits of the error information into a frame currently being encoded ("an error correction encoding circuit 1904 error correction encodes the digital-watermark information 1507 to generate error correction encoding digital-watermark information" at col. 15, line 21), said embedding performed by modifying at least one parameter of the frame currently being encoded ("control unit 1511 can freely set the value of the quantizing step used in the quantizing circuit 1902 in correspondence with the feature of image data for one block. The value of the quantizing step used in the quantizing circuit 1902 is externally supplied as one of the extracting parameter information required" at col. 16, line 2) and extracting the

hidden data including the embedded number of bits provided from the video encoder ("the interpolation detecting unit 2208 decodes the error correction encoding digital-watermark information extracted from each block" at col. 17, line 32),

transmitting the currently encoded frame containing the embedded number of bits ("receives the synthesis image data" at col. 17, line 1) to the video decoder (figure 22); and

extracting the embedded number of bits transmitted from the video encoder at the video decoder (figure 22, numeral 2203).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to utilize the error information embedding and extraction of Hayashi et al. to hide the error frame number in the coded frame of Fukunaga et al. such that the information "can be embedded without deteriorating the original image" (Hayashi et al. at col. 16, line 34).

Regarding **claim 16**, Fukunaga et al. discloses a video communication system wherein the extracted error frame information is an information ("error signal to report all of the erroneous blocks" at col. 6, line 24) that represents whether or not the error occurs in each group of blocks ("multiple blocks in the same frame" at col. 6, line 22).

Regarding **claim 17**, Hayashi et al. discloses that said at least one parameter is at least one of a quantization parameter corresponding to the frame currently being encoded ("control unit 1511 can freely set the value of the quantizing step used in the quantizing circuit 1902 in correspondence with the feature of image data for one block.

The value of the quantizing step used in the quantizing circuit 1902 is externally supplied as one of the extracting parameter information required" at col. 16, line 2) or a level value of a block to which a discrete cosine transform is performed.

Regarding **claim 20**, Hayashi et al. discloses that the data hiding operation is performed before quantization of the frame currently being encoded (as seen in figure 19, the data hiding is performed in 1904 and then proceeds to the quantizer 1902).

8. Claims 9-11, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fukunaga et al., Khansari et al. (US 6,141,448) and Hayashi et al.

Regarding **claim 9**, Fukunaga et al. discloses a video decoder ("decoding apparatus" at col. 13, line 56) comprising:

a decoding processing unit (figure 16, numeral 701) for receiving a compressed video stream ("coded moving-picture data" at col. 5, line 49) from a video encoder ("coding apparatus" at col. 14, line 48) and performing a decoding ("decoding operations" at col. 13, line 61);

a data extraction unit (figure 16, numeral 704) for extracting a hidden data ("copies the relevant blocks of the most recently modified frame" at col. 14, line 42) from the decoded stream, the hidden data being transmitted ("transmit end-of-modification information" at col. 5, line 39) using a data hiding ("frame number is included in the end-of-modification information" at col. 5, line 40) from the video encoder, extracting an information ("frame and block number" at col. 6, line 6) on an error frame ("frame and block number of the block in which the error occurred" at col. 6, line 6), and providing

the extracted frame information to the video encoder ("receives decoding error signals from the decoding apparatus" at col. 4, line 61); and

an error concealment processing unit (figure 16, numeral 702) for performing an error concealment ("error concealment" at col. 14, line 16) with reference to the extracted hidden data ("uses data stored in the concealed-error reference-picture memory 703 for reference" at col. 13, line 62), wherein the hidden data is extracted based on a reference frame included in the compressed video stream ("concealed-error reference-picture memory 703 stores at least the most recent frame supplied by the error concealment unit" at col. 14, line 32).

Fukunaga et al. does not disclose that the decoding unit is a variable length decoding processing unit, that the decoding is a variable length decoding and that the hidden data is based on a number of bits of information embedded in a reference frame, and the number of bits embedded a value of at least one parameter of the reference frame.

Khansari et al. discloses a video decoder ("decoder" at col. 13, line 50) comprising:

a variable length decoding processing unit (figure 14, numeral 520) for receiving a compressed video stream ("coded video stream" at col. 13, line 51) from a video encoder ("encoder" at col. 13, line 51) and performing a variable length decoding ("picture data decoded by variable length decoder" at col. 14, line 1),

wherein hidden data is based on a number of bits of information embedded ("PICTURE/GOB DATA stored in buffer 440 is used by erasure slice constructor 480 to construct the ERASURE SLICE" at col. 13, line 44) in a reference frame ("erasure slice" at col. 9, line 11), and the number of bits embedded a value of at least one parameter of the reference frame ("receives the output of quantizer 420, the PTYPE signal, the INTER/INTRA signal and the motion vectors" at col. 13, line 40).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to utilize the variable length decoder as taught by Khansari et al. to decode the video data of Fukunaga et al. to provide a unit "that it is simple and does not require additional hardware or software to decode the overhead information" (Khansari et al., at col. 7, line 53) and to utilize the slice constructor as taught by Khansari et al. to hide data in the reference frame of Fukunaga et al. to provide a unit wherein the "amount of overhead and delay generated to reconstruct lost information is minimal" (Khansari et al., at col. 7, line 58).

The Fukunaga et al. and Khansari et al. combination does not disclose that the information is error information embedded in the frame.

Hayashi et al. teaches a method in the same field of endeavor of extracting encoded image data ("apparatus for extracting error correction encoding digital-watermark information embedded by the data processing apparatus" at col. 16, line 61) wherein the hidden data is extracted (figure 22, numeral 2203) based on a number of

bits of error information embedded in a frame ("an error correction encoding circuit 1904 error correction encodes the digital-watermark information 1507 to generate error correction encoding digital-watermark information" at col. 15, line 21) and the number of bits embedded a value of at least one parameter ("control unit 1511 can freely set the value of the quantizing step used in the quantizing circuit 1902 in correspondence with the feature of image data for one block. The value of the quantizing step used in the quantizing circuit 1902 is externally supplied as one of the extracting parameter information required" at col. 16, line 2).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to utilize the error information embedding and extraction of Hayashi et al. to hide the error frame number in the coded frame of the Fukunaga et al. and Khansari et al. combination such that the information "can be embedded without deteriorating the original image" (Hayashi et al. at col. 16, line 34).

Regarding **claim 10**, Hayashi et al. discloses that the hidden data is extracted during an inverse quantization ("dequantizes the predetermined coefficient information...thus extracting 1-bit embedded information" at col. 17, line 28).

Regarding **claim 11**, Hayashi et al. discloses that said at least one parameter is at least one of a quantization parameter corresponding to the frame currently being encoded ("control unit 1511 can freely set the value of the quantizing step used in the quantizing circuit 1902 in correspondence with the feature of image data for one block. The value of the quantizing step used in the quantizing circuit 1902 is externally

supplied as one of the extracting parameter information required" at col. 16, line 2) or a level value of a block to which a discrete cosine transform is performed.

Regarding **claim 13**, Fukunaga et al. discloses a video decoder wherein the extracted frame information is an information ("error signal to report all of the erroneous blocks" at col. 6, line 24) that represents whether or not the error occurs in each GOB ("multiple blocks in the same frame" at col. 6, line 22).

9. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fukunaga et al., Hayashi et al. and common knowledge in the art as applied to claim 1 above, and further in view of Lin et al. (US 2002/0141502).

Regarding **claim 5**, the combination of Fukunaga et al., Hayashi et al. and common knowledge in the art disclose the elements of claim 1 as described in the 103 rejection above.

The combination of Fukunaga et al., Hayashi et al. and common knowledge in the art does not disclose that the video encoder performs the data hiding using a quantization parameter with respect to an encoding video image or a level value of a block to which a discrete cosine transform is performed.

Lin et al. discloses a video coding method wherein the video encoder ("compressor" at paragraph 0029, line 1) performs the data hiding ("introduce the error-detection information into the bitstream" at paragraph 0031, line 2) wherein the at least one parameter is a level value ("quantized DCT coefficients" at paragraph 0031, line 1)



of a block ("each block" at paragraph 0028, line 1) to which a discrete cosine transform ("discrete cosine transform" at paragraph 0029, line 3) is performed.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to utilize the level value as taught by Lin et al. to hide the error data of the combination of Fukunaga et al. and common knowledge in the art to provide an encoder that "improves the compression ratio" (Lin et al., at paragraph 0030, line 8).

Regarding **claim 6**, Lin et al. discloses that the level value is a value obtained by dividing a discrete cosine coefficient by the quantization parameter (figure 3, numeral 126).

10. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fukunaga et al., Hayashi et al. and common knowledge in the art as applied to claim 1 above, and further in view of Bannon et al. (US 6,272,253).

Regarding **claim 7**, the combination of Fukunaga et al., Hayashi et al. and common knowledge in the art discloses the elements of claim 1 as described in the 103 rejection above.

The combination of Fukunaga et al., Hayashi et al. and common knowledge in the art does not disclose that the error concealment is performed by calculating average of motion vectors of blocks surrounding an error block and performing motion compensation to a reference frame.

Bannon et al. discloses a video communication system ("digital communication and storage systems with compressed video" at col. 1, line 6) wherein error

concealment ("Error Concealment" at col. 9, line 62) is performed by calculating average of motion vectors of blocks ("Average the motion vectors over all macroblocks within the region" at col. 9, line 56) surrounding an error block ("error is detected in the motion vector data" at col. 18, line 22) and performing motion compensation ("motion compensation techniques" at col. 10, line 4) to a reference frame ("previous reconstructed frame" at col. 9, line 21).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to utilize the motion estimation and compensation as taught by Bannon et al. to conceal the error data of the combination of Fukunaga et al., Hayashi et al. and common knowledge in the art to provide a result with "good approximation and help reduce visual distortion significantly" (Bannon et al., at col. 18, line 29).

Regarding **claim 8**, Bannon et al. discloses a video communication system wherein the surrounding blocks ("each 16 by 16 macroblock in  $F_N$  which corresponds to a macroblock indicated by the bit map to be within the region" at col. 9, line 18) for obtaining the average of the motion vectors are upper and lower blocks (upper and lower blocks of the search area which "extends 15 pixels in all directions" at col. 9, line 29) of a block in which the error occurs.

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fukunaga et al., Khansari et al. and Hayashi et al. as applied to claim 9 above, and further in view of Bannon et al.

The combination of Fukunaga et al., Khansari et al. and Hayashi et al. discloses the elements of claim 9 as described in the 103 rejections above.

The combination of Fukunaga et al., Khansari et al. and Hayashi et al. does not disclose that the error concealment is performed by calculating average of motion vectors of blocks surrounding an error block and performing motion compensation to a reference frame.

Bannon et al. discloses a video communication system ("digital communication and storage systems with compressed video" at col. 1, line 6) wherein error concealment ("Error Concealment" at col. 9, line 62) is performed by calculating average of motion vectors of blocks ("Average the motion vectors over all macroblocks within the region" at col. 9, line 56) surrounding an error block ("error is detected in the motion vector data" at col. 18, line 22) and performing motion compensation ("motion compensation techniques" at col. 10, line 4) to a reference frame ("previous reconstructed frame" at col. 9, line 21).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to utilize the motion estimation and compensation as taught by Bannon et al. to conceal the error data of the combination of Fukunaga et al., Khansari et al. and Hayashi et al. to provide a result with "good approximation and help reduce visual distortion significantly" (Bannon et al., at col. 18, line 29).

12. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fukunaga et al. and Hayashi et al. as applied to claim 15 above, and further in view of Bannon et al.

The combination of Fukunaga et al., and Hayashi et al. discloses the elements of claim 1 as described in the 103 rejection above.

The combination of Fukunaga et al., and Hayashi et al. does not disclose that the error concealment is performed by calculating average of motion vectors of blocks surrounding an error block and performing motion compensation to a reference frame.

Bannon et al. discloses a video communication system ("digital communication and storage systems with compressed video" at col. 1, line 6) wherein error concealment ("Error Concealment" at col. 9, line 62) is performed by calculating average of motion vectors of blocks ("Average the motion vectors over all macroblocks within the region" at col. 9, line 56) surrounding an error block ("error is detected in the motion vector data" at col. 18, line 22) and performing motion compensation ("motion compensation techniques" at col. 10, line 4) to a reference frame ("previous reconstructed frame" at col. 9, line 21).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to utilize the motion estimation and compensation as taught by Bannon et al. to conceal the error data of the combination of Fukunaga et al., and Hayashi et al. to provide a result with "good approximation and help reduce visual distortion significantly" (Bannon et al., at col. 18, line 29).

### ***Response to Arguments***

13. Applicant's arguments with respect to claims 1, 3-11 and 13-20 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

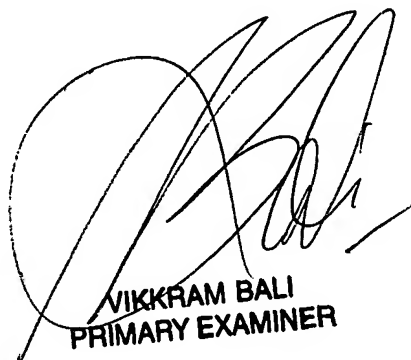
15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Katrina Fujita whose telephone number is (571) 270-1574. The examiner can normally be reached on M-Th 8-5:30pm, F 8-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vikkram Bali can be reached on (571) 272-7415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Katrina Fujita  
Art Unit 2624



VIKKRAM BALI  
PRIMARY EXAMINER